IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Docket No.: **TI-34776**
Khurram Muhammad	Art Unit: **2816**
Serial No.: **10/712,593**	Examiner: **Le, Dinh Tranh**
Filed: **11/13/2003**	Conf. No.: **8991**

For: **A TECHNIQUE FOR IMPROVING ANTIALIASING AND ADJACENT CHANNEL INTERFERENCE FILTERING USING CASCADED PASSIVE IIR FILTER STAGES COMBINED WITH DIRECT SAMPLING AND MIXING**

SUBSTITUTE APPELLANTS' BRIEF – 37 C.F.R. § 1.192(c)

Commissioner for Patents
Alexandria, VA 22313-1450

Dear Sir:

This Appeal Brief is submitted in connection with the above-identified application in response to the final Office Action mailed August 8, 2007 and the Office communication mailed November 29, 2007.

I. REAL PARTY IN INTEREST

Texas Instruments Incorporated is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Appellants are aware of a pending appeal in related application 11/388,558. An Appeal Brief in the related application was filed on October 24, 2007.

III. STATUS OF CLAIMS

Claims 2-20, 24-35, 37-40 are pending in the application. Claims 1, 21-23 and 36 are canceled. Claims 5, 9-15, 17-20, 25, 27, 29-35 and 37-40 are allowed. Objected to Claim 3 was amended to be in allowable form in an Amendment under 37 CFR 1.116 submitted on November 14, 2007 to place Claim 3 in condition for allowance. Appellants assume there will be no problem entering the amendment. Final Rejection of Claims 2-4, 6-8, 16, 24, 26 and 28 was made by the Examiner in the Office Action dated August 8, 2007. Claims 2, 4, 6-8, 16, 24, 26 and 28 are on appeal. Claims 2, 4, 6-8, 16, 24, 26 and 28 are reproduced in the Appendix to Appellants' Brief filed herewith.

Appellants note for the record that Claim 26 should be substituted for Claim 25 in the "Claims Rejected" category since Claim 25 is allowed and already identified in the "Claims Allowed" category.

IV. STATUS OF AMENDMENTS

An Amendment under 37 CFR § 1.116 was submitted to the USPTO on October 22, 2007. In an Advisory Action dated November 2, 2007, Examiner states that the Amendment will be entered for the purposes of appeal.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention discloses a technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages (100, 110, 112) combined with direct sampling and mixing (Fig. 3; page 6, line 13 – page 9, line 10). The methodology and related architecture provides increased passive IIR filtering without necessitating use of amplifier stages.

Claim 4 requires and positively recites, a high order filter comprising: "a cascade of single pole IIR filters configured to generate an output signal in response to an input signal (Fig. 3, 100, 110, 112; page 6, line 13- page 9, line 10)", "means for direct sampling (See the LNTA connected to CH(104) through the mixer switch driven by LO in FIGS. 1 and 2. The (two) first sampling switches following the CH are the means for direct sampling – and are not assigned an identifier number. These switches have BANK1 and BANK2 written under them) coupled to the cascade of single pole IIR filters" and "at least one amplifier stage (amplifer following PIIR (100) in FIG. 4B – not assigned a identifier number) coupled to the cascade of single pole IIR filters".

Claim 16 requires and positively recites, a discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal (Fig. 3, 100, 110, 112; page 6, line 13- page 9, line 10), wherein the single pole IIR filters are comprised solely of switches and capacitors".

Claim 24 requires and positively recites, a receiver front-end comprising: "a cascade of single pole IIR filters configured to generate an output signal in response to an input signal (Fig. 3, 100, 110, 112; page 6, line 13- page 9, line 10)", "means for direct sampling coupled to the cascade of single pole IIR filters (See the LNTA connected to

CH(104) through the mixer switch driven by LO in FIGS. 1 and 2. The (two) first sampling switches following the CH are the means for direct sampling – and are not assigned an identifier number. These switches have BANK1 and BANK2 written under them)" and "at least one amplifier stage (amplifer following PIIR (100) in FIG. 4B – not assigned a identifier number) coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter".

Claim 28 requires and positively recites, a receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal (Fig. 3, 100, 110, 112; page 6, line 13- page 9, line 10), wherein the cascade of single pole IIR filters comprises a history capacitor (C_H) coupled to a first rotating capacitor (C_{R1}) in a first capacitor bank (BANK 1).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Are Claims 2, 4, 6, 7, 16, 24 and 26 patentable under 35 U.S.C. 102(b) over Yasuda (US 6,181,740)?

2) Are Claims 8, 16 and 28 patentable under 35 U.S.C. 102(b) over Arvidsson et al. (US 6,414,541).

VII. ARGUMENTS

1) Claims 2, 4, 6, 7, 16, 24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasuda (US 6,181,740). Appellants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 2, 4, 6, 7, 16, 24 and 26 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 4 requires and positively recites a high order filter comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**".

Independent Claim 16 requires and positively recites, a discrete time analog filter comprising a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **single pole IIR filters** are comprised solely of switches and capacitors.

Independent Claim 24 requires and positively recites, a receiver front-end comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**, wherein the cascade of **single pole IIR filters**, the means for direct sampling, and the at least one amplifier stage together implement a high order filter".

In contrast, Yasuda discloses a sampling system that embeds an analog decimation filter composed of an FIR filter (col. 2, lines 33-48; col. 3, lines 20-30) having the purpose of providing anti-alias filtering to noise folding inherent in sub-sampling receivers. While a filter can be realized using capacitors and switches only, Yasuda discloses a finite-impulse response filter design that is obtained by combining weighted sum of input samples in a window of n samples (sampled on C11 to C1n) to obtain anti-aliasing filtering for noise folding due to decimation. This is clearly described in the Abstract and in the Body of the specification. Each time C11 to C1n sample the input, the arrangement cannot provide an infinite-impulse response, which relies on a sampler that maintains the history of sampled charge for infinite previous samples as in suggested in our proposal.

Yasuda does not provide any means for integration of previous samples on the sampling capacitors, since the sampling capacitor is driven by a LNA through a bandpass filter, that presents an input voltage that is sampled on to the sampling capacitor. Of course n samples can be sampled and combined together when presented to the summing amplifier, however, the response is FIR followed immediately by decimation by n, since 1 output is produced for every n inputs. The weighting of individual samples can be done as shown in FIG. 8, however, the system can only provide FIR response, since there is no means for accumulating samples in an infinite window. Therefore, Appellants respectfully disagree with Examiner's determination that Yasuda suggests an IIR filter, since an IIR

filter must have a memory element that maintains some information of all the previous samples, hence providing an infinite impulse response.

Accordingly, Yasuda does not disclose or even remotely suggest an IIR filter in Figures 3 or 9 which only show sample-and-hold circuits sampling input voltage (see col. 10, lines 50 onwards), providing an input to a sigma-delta A/D converter that accepts the input from the plurality of these sample-and-hold circuits. Nothing disclosed in Yasuda provides IIR filtering function. Even if FIR filtering could be achieved in Yasuda by combining samples as they are sampled to the input of the A/D converter (see col. 11), sampling n consecutive samples on n distinct capacitors and combining a weighted average of these would not provide an IIR response! One window of n samples does not affect the output produced by the next window of n samples. IIR filtering is neither anticipated by Yasuda, not implied or remotely suggested. No means are provided in Yasuda to achieve such a response.

Accordingly, Yasuda fails to teach or suggest, a high order filter comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**", as required by Claim 4 OR a discrete time analog filter comprising a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **single pole IIR filters** are comprised solely of switches and capacitors, as required by Claim 16, OR a receiver front-end comprising: "a cascade of **single pole IIR filters** configured to generate an output signal in response to an input signal", "means for direct sampling coupled to the cascade of **single pole IIR filters**" and "at least one amplifier stage coupled to the cascade of **single pole IIR filters**, wherein the cascade of **single pole IIR filters**, the means for direct sampling, and the at least one amplifier stage together

implement a high order filter", as required by Claim 24. The 35 U.S.C. 102(b) rejection of Claims 4, 16 and 24 is improper and must be reversed.

Claims 2, 6, 7 and 26 stand allowable as depending from allowable claims and by including further limitations not taught or suggested by Yasuda.

Claim 2 further defines the discrete time analog filter according to claim 16, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers. Claim 2 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 6 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers. Claim 6 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 7 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage. Claim 7 depends from Claim 16 and is allowable for the same reasons set forth above in support of the allowance of Claim 16.

Claim 26 further defines the receiver front-end according to claim 24, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers. Claim 26 depends from Claim 24 and is allowable for the same reasons set forth above in support of the allowance of Claim 24.

2) Claims 8, 16 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Arvidsson et al. (US 6,414,541). Appellants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 8, 16 and 28 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." *Verdegall Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 16, requires and positively recites a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors.**

Independent Claim 28 requires and positively recites, a receiver front-end comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **cascade of single pole IIR filters** comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

In contrast, Arvidsson does not propose cascading IIR filters. Arvidsson discloses only one stage of IIR filter as explained by the recursive equation in col. 1, line 32. In his disclosure, Arvidsson proposes a means for sampling an input on C1 together with a rotating capacitor. Arvidsson then disconnects the rotating capacitor from the input and

shows a means for multiplying the sample on the rotating capacitor by a factor less than 1, thereby providing an increased resolution, that would otherwise be only obtainable by placing numerous equal-sized part capacitors as he explains in col. 1 in the BACKGROUND section.

C1-C6 do not provide a filter pole, as suggested by Examiner. On the contrary, C1-C6 provide a means for dividing the input sample to obtain a fractional-sample to help realize a higher resolution that would otherwise be only available using a large bank of sampling capacitor.

As such, Arvidsson provides no teaching of cascading filter stages. Arvidsson similarly provides no teaching of maintaining a constant rate of information flow through cascaded filter stages. Appellants note that C2-C6 also show reset switches, while C1 has no reset switch. Hence, CB1 or CB2 are not implied, or suggested, since the "memory" of previous inputs must be maintained by a sampling capacitor that is never discharged in order to obtain an IIR response. For cascaded filtering stages, there must me more than one capacitor that is never reset such as the case with CB1 and CB2 in the present application. A constant rate of information flow must be maintained, and hence, at least two rotating capacitors are needed to transport charge from one stage to the next.

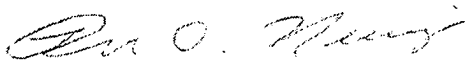
Accordingly, Ardvidson fails to teach or suggest, a discrete time analog filter comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, **wherein the single pole IIR filters are comprised solely of switches and capacitors**, as required by Claim 16 OR a receiver front-end comprising a **cascade of single pole IIR filters** configured to generate an output signal in response to an input signal, wherein the **cascade of single pole IIR filters** comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank, as required by Claim 28.

Accordingly, the 35 U.S.C. 102(b) rejection of Claims 16 and 28 is improper and must be reversed.

Claim 8 further defines the discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank. Claim 8 depends from Claim 16 and stands allowable for the same reasons Claim 16 is allowable.

For the above reasons, favorable consideration of the appeal of the Final Rejection in the above-referenced application, and its reversal, are respectfully requested.

Respectfully submitted,



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CLAIMS APPENDIX

CLAIMS ON APPEAL:

1. (Canceled)

2. The discrete time analog filter according to claim 16, further comprising means for direct sampling, wherein the cascade of single pole IIR filters and means for direct sampling together implement a high order filter devoid of amplifiers.

3. (Allowed)

4. A high order filter comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

means for direct sampling coupled to the cascade of single pole IIR filters;~~,~~ and

at least one amplifier stage coupled to the cascade of single pole IIR filters.

5. (Allowed)

6. The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers.

7. The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters is operational to create a uni-directional flow of information, signal, or charge and disallow any feedback from a later filter stage to an earlier filter stage.

8. The discrete time analog filter according to claim 16, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

9-15. (Allowed)

16. A discrete time analog filter comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the single pole IIR filters are comprised solely of switches and capacitors.

17-20. (Allowed)

21-23. (Canceled)

24. A receiver front-end comprising:

a cascade of single pole IIR filters configured to generate an output signal in response to an input signal;

means for direct sampling coupled to the cascade of single pole IIR filters; and

at least one amplifier stage coupled to the cascade of single pole IIR filters, wherein the cascade of single pole IIR filters, the means for direct sampling, and the at least one amplifier stage together implement a high order filter.

25. (Allowed)

26. The receiver front-end according to claim 24, wherein the cascade of single pole IIR filters together implement a high order filter devoid of amplifiers.

27. (Allowed)

28. A receiver front-end comprising a cascade of single pole IIR filters configured to generate an output signal in response to an input signal, wherein the cascade of single pole IIR filters comprises a history capacitor coupled to a first rotating capacitor in a first capacitor bank.

29-35. (Allowed)

36. (Canceled)

37-40. (Allowed)

RELATED PROCEEDINGS APPENDIX

Appellants are aware of a pending appeal in related application 11/388,558. An Appeal Brief in the related application was filed on October 24, 2007.

EVIDENCE APPENDIX

No documents are being submitted with the Appeal Brief.